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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/890,214	05/31/2002	Masaru Yasui	PHJ 99-026	8898

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EXAMINER

NATNAEL, PAULOS M

ART UNIT	PAPER NUMBER
2622	

2622

DATE MAILED: 07/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No. 09/890,214	Applicant(s) YASUI ET AL.	
Examiner Paulos M. Natnael	Art Unit 2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 5/4/06 and phone interview of 7/10/06.
- 2a) This action is **FINAL**.
- 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-15 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) 5-7,9,13 and 15 is/are allowed.
- 6) Claim(s) 1-3,8,10 and 14 is/are rejected.
- 7) Claim(s) 4,11 and 12 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 31 May 2002 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

DETAILED ACTION

1. The Final Rejection mailed on May 10, 2006 has been withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims **1,3,8** are again rejected under 35 U.S.C. 102(e) as being anticipated by **Hashimoto et al. U.S. 6,072,457.**

Considering claim 1, Hashimoto et al (hereinafter, Hashimoto) discloses a display and driving method comprising at least two line memories (100-2, 100-1, fig.2) a control circuit 140 and at least a couple of signal processors, 120-1 and 120-2. On col. 11, line 45 thru col. 12, line 10 and referring to Figure 15, Hashimoto teaches that “The writing into and the reading from the line memory are performed in the following order. First, upon a start signal 26 of the shift register 4 at the writing side, the shift register 4 starts the operation, making sampling 1200 times during one horizontal scan period, and sequentially writing into the line memory. At the time when the sampling (600+6) times

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or more is ended, upon a start signal 28 of the shift register 18 at the reading side, the operation of the shift register 18 if started, so that data at the odd address is read in the order of 1, 3, 5 addresses (Ro1, Go1, Bo1), and 7, 9, 11 addresses (Ro2, Go2, Bo2) of the line memory, three data at the same time. If the frequency of read clock at this time is three times that of the write clock, the reading up to the (1200-6)-th address has been performed at the time when the writing into the line memory is ended, whereby the reading is not performed before the writing into the line memory. Also, the reading is performed within $t_{sub.H} / 2$ which is half one horizontal scan period $t_{sub.H}$, while the writing into the first row of the liquid crystal panel is ended. During the next $t_{sub.H} / 2$ period, data at the even address is read, three data at the same time, in the order of 2, 4, 6 addresses (Be1, Re1, Ge1), 8, 10, 12 addresses (Be2, Re2, Ge2), . . . in the same manner as above described. Then, the sampling of image signal for the next horizontal scan period is performed, and data is written into the line memory, but the order of the writing and reading is not reversed if the reading precedes the writing. Where the reading of data is performed after the end of the writing into the line memory, a line memory for the image signal during two horizontal scan periods is required, but by reading the image signal data from the line memory while writing into the same line memory, as in this example, the line memory can be halved." [emphasis added by examiner] Thus, the claimed subject matter in claim 1 is met by the disclosure of Hashimoto as shown above.

Regarding claim 3, see rejection of claim 1 and the display and driving methods of Hashimoto illustrated therein.

As to claim 8, see rejection of claim 1;

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims **2,10, and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto, U.S. 6,072457.

Considering claims **2,14**, Hashimoto discloses line memories without specifying whether the line memories are also dual port and/or FIFOs. However, the examiner takes Official Notice in that dual port memories and FIFOs in signal conversion or interpolation circuits are notoriously well known in the art of television, and it would have been obvious to the skilled in the art at the time the invention was made to modify the reference of Hashimoto by providing a dual port FIFO type memory device in order to more efficiently write and read video information to and from the memories to efficiently interpolate the signals as desired.

As to claim 10, see rejection of claim 3.

Response to Arguments

6. Applicant's arguments filed 11-14-05 have been fully considered but they are not persuasive. Applicant argues that the quoted passage (col. 11, line 45 thru col. 12, line 10) only discloses one line memory and thus, the applicant asserts, the reference does not teach two line memories as claimed.

Contrary to the Applicant's assertion, however, the reference of "Hashimoto" teaches on col. 12, starting on line 5, "Where the reading of data is performed after the end of the writing into the line memory, a line memory for the image signal during two horizontal scan periods is required, but by reading the image signal data from the line memory while writing into the same line memory, as in this example, the line memory can be halved." Clearly, since both writing and reading from the same memory simultaneously would be difficult to do, Hashimoto suggests a solution and the line memory can be halved, yielding, as it were, two line memories. Thus, the disclosure of Hashimoto as a whole meets the claim as claimed.

In response to applicant's demand for the showing of an evidence to support the taking of Official Notice (Record of Telephonic Interview, May 4, 2006), the examiner presents Yoshida, U.S. Pat. No. 5,168,362. One of the objectives of the invention is claimed to be displaying efficiently interpolated image to any size on the screen through the use of a memory device. See Summary of the Invention (page 2) of the instant application. Yoshida discloses an apparatus for displaying standard aspect ratio [such

as 4:3] television signal on wide aspect ratio display screen [such as 16:9]. In Fig.6, Yoshida discloses an arrangement of an aspect ratio converting circuit comprising the dual port line memory 23, which memory is described on col. 7, lines 23-26, as a FIFO type memory. Thus, as evidenced by the disclosure of Yoshida, dual mode FIFO memories in signal interpolation or conversion are notoriously well-known in the art.

Allowable Subject Matter

7. Claims 5-7,9,13,15 are allowable over the prior art.
8. Claims 4,11-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

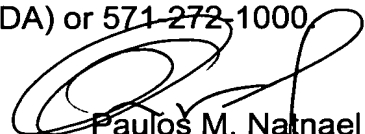
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (571) 272-7354. The examiner can normally be reached on 9am - 5:30pm M,W, F (7am-3:30pm T,Th).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Paulos M. Natnael
Primary Examiner
Art Unit 2622

PMN
July 10, 2006